In re Patent Application of
KAUSHIK ET AL.
Serial No. **10/662,952**
Filed: **SEPTEMBER 12, 2003**

In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

1. (currently amended) An output buffer comprising:

~~supply~~ voltage terminals;

an output stage including multiple, independently controllable output switches;

an output driver stage providing a control signal for the output stage; and

a correcting stage monitoring a ~~supply~~ voltage of at least one of the ~~supply~~ voltage terminals in view of the control signal, and dynamically controlling at least one of the controllable output switches so as to provide rapid response while limiting a ~~supply~~ voltage bounce at the ~~supply~~ voltage terminals within a predefined limit, the correcting stage including

a first feedback switch connected between the output driver stage and the at least one controllable output switch,

an inverter connected between the at least one voltage terminal and a control terminal of the first feedback switch, the inverter having a trip point controlled by the voltage on the at least one voltage terminal, and

a second feedback switch connected between the at least one voltage terminal and the at least one controllable output switch.

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2. (currently amended) An output buffer according to Claim 1 wherein the correcting stage disables the at least one ~~selected~~ controllable output switch~~es~~ via the inverter whenever a sensed ~~supply~~ voltage bounce increases beyond ~~a predefined threshold level~~ the trip point and enables the at least one ~~selected~~ controllable output switch~~es~~ whenever the sensed ~~supply~~ voltage bounce falls below the ~~threshold voltage level~~ trip point.

3. (Original) An output buffer according to Claim 1 wherein the independently controllable output switches comprise switching transistors having output terminals connected together, and at least one of the switching transistors has a control terminal operated by the correcting stage.

4. (Original) An output buffer according to Claim 3 wherein the switching transistors comprise MOS transistors.

5. (Original) An output buffer according to Claim 4 wherein the MOS transistors are sized in a binary-weighted sequence.

6. (currently amended) An output buffer comprising:

~~supply~~ voltage terminals;

an output stage including a plurality of independently controllable switching transistors having output terminals connected together;

an output driver stage providing a control signal for the output stage; and

a correcting stage monitoring a ~~supply~~ voltage of at least one of the ~~supply~~ voltage terminals, and controlling at least one of the controllable switching transistors to limit a ~~supply~~ voltage bounce at the ~~supply~~ voltage terminals within a predefined limit, the correcting stage including

a first feedback switch connected between the output driver stage and the at least one controllable switching transistor,

an inverter connected between the at least one voltage terminal and a control terminal of the first feedback switch, the inverter having a trip point controlled by the voltage on the at least one voltage terminal, and

a second feedback switch connected between the at least one voltage terminal and the at least one controllable switching transistor.

7. (currently amended) An output buffer according to Claim 6 wherein the correcting stage disables the at least one ~~selected~~ controllable switching transistor~~s~~ whenever a sensed ~~supply~~ voltage bounce increases beyond ~~a predefined threshold level~~ the trip point and enables the at least one ~~selected~~ controllable switching transistor~~s~~ whenever the

sensed ~~supply~~ voltage bounce falls below the ~~threshold voltage level~~ trip point.

8. (Original) An output buffer according to Claim 6 wherein at least one of the switching transistors has a control terminal operated by the correcting stage.

9. (Original) An output buffer according to Claim 8 wherein the switching transistors comprise MOS transistors.

10. (Original) An output buffer according to Claim 9 wherein the MOS transistors are sized in a binary-weighted sequence.

11. (currently amended) A method for reducing ~~supply~~ voltage bounce while maintaining speed of operation of an output buffer comprising:

providing multiple, independently controllable output switches in an output stage of the output buffer;

providing a control signal to the output stage from an output driver stage; and

monitoring a voltage of at least one ~~supply~~ terminal, with a correcting stage, whenever ~~an input~~ the control signal changes state and dynamically controlling at least one of the controllable output switches so as to provide rapid response while limiting a ~~supply~~ voltage bounce at the ~~supply~~ terminals within a predefined limit, the correcting stage including

a first feedback switch connected between the output driver stage and the at least one controllable output switch,

an inverter connected between the at least one voltage terminal and a control terminal of the first feedback switch, the inverter having a trip point controlled by the voltage on the at least one voltage terminal, and

a second feedback switch connected between the at least one voltage terminal and the at least one controllable output switch.

12. (currently amended) A method according to Claim 11 wherein the correcting stage disables the at least one ~~selected~~ controllable output switches whenever a sensed ~~supply~~ voltage bounce increases beyond ~~a predefined threshold level~~ the trip point and enables the at least one ~~selected~~ controllable output switches whenever the sensed ~~supply~~ voltage bounce falls below the ~~threshold voltage level~~ trip point.

13. (currently amended) A method for reducing ~~supply~~ voltage bounce while maintaining speed of operation of an output buffer comprising:

providing a plurality of independently controllable switching transistors having output terminals connected together in an output stage of the output buffer;

providing a control signal for the output stage; and

monitoring a voltage of at least one ~~supply~~ terminal, with a correcting stage, whenever the control signal changes state and dynamically controlling at least one of the controllable switching transistors to limit ~~supply~~ voltage bounce at the ~~supply~~ terminals within a predefined limit, the correcting stage including

a first feedback switch receiving the control signal and connected to the at least one controllable switching transistor,

an inverter connected between the at least one voltage terminal and a control terminal of the first feedback switch, the inverter having a trip point controlled by the voltage on the at least one voltage terminal, and

a second feedback switch connected between the at least one voltage terminal and the at least one controllable switching transistor.

14. (currently amended) A method according to Claim 13 wherein the correcting stage disables the at least one ~~selected~~ controllable switching transistor~~s~~ whenever a sensed ~~supply~~ voltage bounce increases beyond ~~a predefined threshold level~~ the trip point and enables the at least one ~~selected~~ controllable switching transistor~~s~~ whenever the sensed ~~supply~~ voltage bounce falls below the ~~threshold voltage level~~ trip point.

15. (Original) A method according to Claim 14 wherein at least one of the switching transistors has a control terminal operated by the correcting stage.

16. (Original) A method according to Claim 14 wherein the switching transistors comprise MOS transistors.

17. (Original) A method according to Claim 16 wherein the MOS transistors are sized in a binary-weighted sequence.